

# **BSS84**

# P-channel enhancement mode vertical D-MOS transistor Rev. 04 — 17 July 2007 Product data

**Product data sheet** 

# **Product profile**

## 1.1 General description

P-channel enhancement mode vertical D-MOS transistor in a SOT23 Surface-Mount Device (SMD) package.

## 1.2 Features

- Low threshold voltage
- High-speed switching
- Direct interface to CMOS and Transistor-Transistor Logic (TTL)
- No secondary breakdown

## 1.3 Applications

■ Line current interrupter in telephone sets ■ Relay, high-speed and line transformer drivers

## 1.4 Quick reference data

- $V_{DS} \le -50 \text{ V}$
- $\blacksquare$  R<sub>DSon</sub>  $\leq$  10  $\Omega$

- $I_D \le -130 \text{ mA}$
- Arr P<sub>tot</sub>  $\leq$  250 mW

# **Pinning information**

#### Table 1. **Pinning**

Pin	Description	Simplified outline	Symbol
1	gate (G)	<u> </u>	
2	source (S)		D
3	drain (D)	1	G
			001aaa025



#### P-channel enhancement mode vertical D-MOS transistor

# 3. Ordering information

Table 2. Ordering information

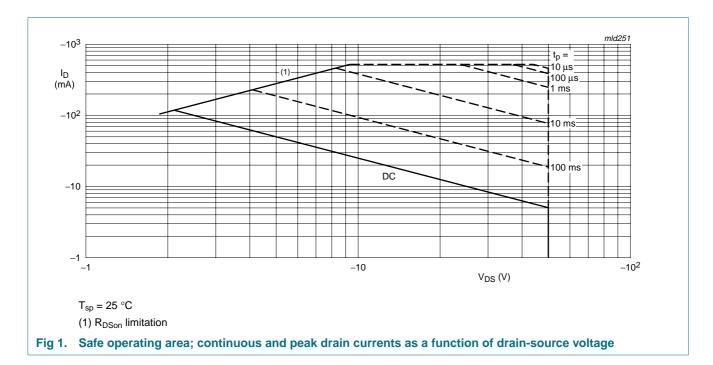
Type number	Package		
	Name	Description	Version
BSS84	TO-236AB	plastic surface-mounted package; 3 leads	SOT23

# 4. Limiting values

## Table 3. Limiting values

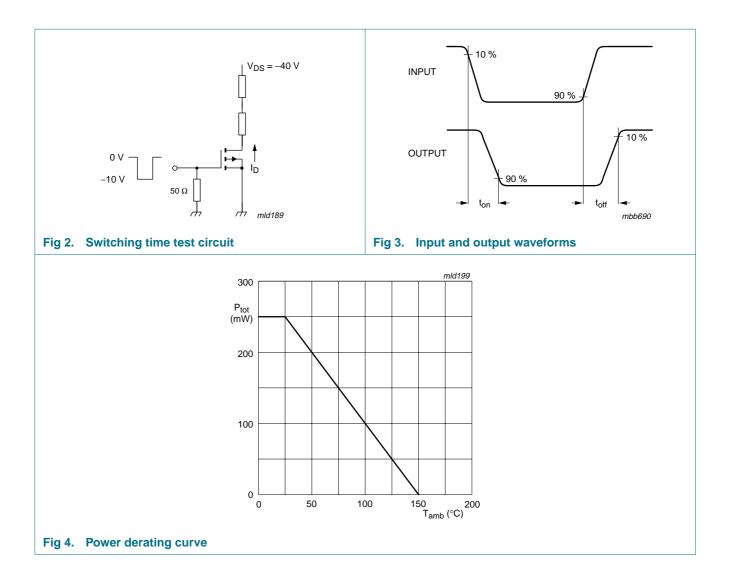
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25  {}^{\circ}\text{C} \le T_j \le 150  {}^{\circ}\text{C}$	-	-50	V
$V_{GS}$	gate-source voltage		-	±20	V
$I_D$	drain current	$T_{sp} = 25 ^{\circ}\text{C}$ ; $V_{GS} = -10 \text{V}$ ; see Figure 1	-	-130	mΑ
		$T_{sp} = 100 ^{\circ}\text{C};  V_{GS} = -10 ^{\circ}\text{V}$	-	<b>-75</b>	mΑ
$I_{DM}$	peak drain current	$T_{sp}$ = 25 °C; pulsed; $t_p \le 10 \mu s$ ; see Figure 1	-	-520	mΑ
P <sub>tot</sub>	total power dissipation	T <sub>sp</sub> = 25 °C; see <u>Figure 4</u>	-	250	mW
T <sub>stg</sub>	storage temperature		-65	+150	°C
Tj	junction temperature		-65	+150	°C



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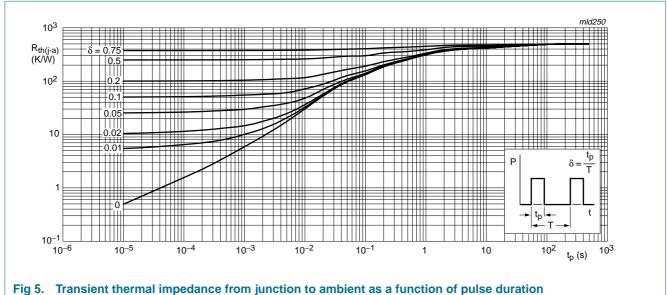
#### P-channel enhancement mode vertical D-MOS transistor

## Thermal characteristics

Table 4. **Thermal characteristics** 

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	see Figure 5	<u>[1]</u> _	-	500	K/W

[1] Mounted on a printed-circuit board; vertical in still air



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# 6. Characteristics

Table 5. Characteristics

 $T_j = 25 \,^{\circ}C$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static ch	naracteristics					
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	$I_D = -10 \mu A; V_{GS} = 0 V$				
		T <sub>j</sub> = 25 °C	-50	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	$I_D = -1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; see Figure 10				
		T <sub>j</sub> = 25 °C	-0.8	-	-2	V
		T <sub>j</sub> = −55 °C	-	-	-1.8	V
I <sub>DSS</sub>	drain leakage current	$V_{DS} = -40 \text{ V}; V_{GS} = 0 \text{ V}$				
		T <sub>j</sub> = 25 °C	-	-	-100	nA
		$V_{DS} = -50 \text{ V}; V_{GS} = 0 \text{ V}$				
		T <sub>j</sub> = 25 °C	-	-	-10	μΑ
		T <sub>j</sub> = 125 °C	-	-	-60	μΑ
I <sub>GSS</sub>	gate leakage current	$V_{GS} = \pm 20 \text{ V}; V_{DS} = 0 \text{ V}$	-	-	±100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -10 \text{ V}; I_D = -130 \text{ mA}; \text{ see } \frac{\text{Figure 7}}{\text{and } 9}$				
		T <sub>j</sub> = 25 °C	-	6	10	Ω
Dynamic	characteristics					
Y <sub>fs</sub>	transfer admittance	$V_{DS} = -25 \text{ V}; I_{D} = -130 \text{ mA}$	50	-	-	mS
C <sub>iss</sub>	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = -25 \text{ V}; f = 1 \text{ MHz};$	-	25	45	pF
Coss	output capacitance	see Figure 11	-	15	25	pF
C <sub>rss</sub>	reverse transfer capacitance		-	3.5	12	pF
t <sub>on</sub>	turn-on time	$V_{DS} = -40 \text{ V}; V_{GS} = 0 \text{ V to } -10 \text{ V};$ $I_D = -200 \text{ mA}; \text{ see } \frac{\text{Figure 2}}{\text{MS}} = \frac{3}{100} \text{ M};$	-	3	-	ns
t <sub>off</sub>	turn-off time	$V_{DS} = -40 \text{ V}; V_{GS} = -10 \text{ V} \text{ to } 0 \text{ V};$ $I_D = -200 \text{ mA}; \text{ see } \frac{\text{Figure 2}}{\text{Joseph Model}} \text{ and } \frac{3}{\text{Joseph Model}}$	-	7	-	ns

## P-channel enhancement mode vertical D-MOS transistor

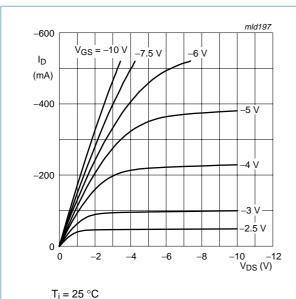
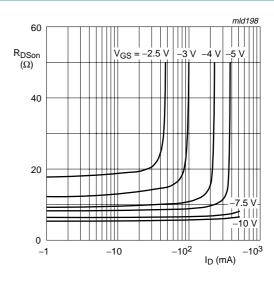


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



T<sub>i</sub> = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values

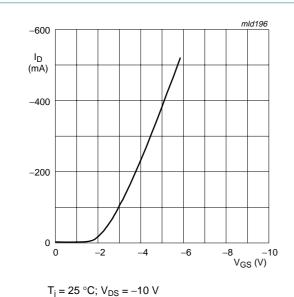
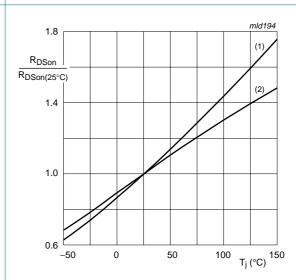


Fig 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values



(1)  $I_D = -130 \text{ mA}$ ;  $V_{GS} = -10 \text{ V}$ 

(2)  $I_D = -20 \text{ mA}$ ;  $V_{GS} = -2.4 \text{ V}$ 

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature

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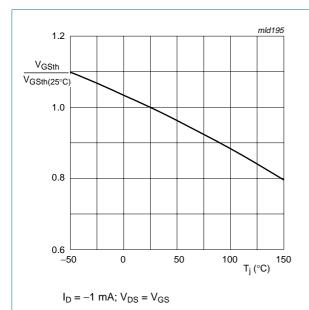
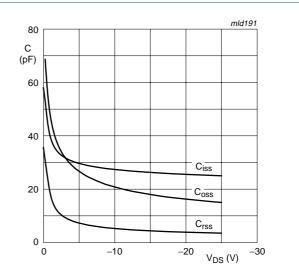


Fig 10. Gate-source threshold voltage as a function of junction temperature



 $V_{GS} = 0 V$ ; f = 1 MHz

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

#### P-channel enhancement mode vertical D-MOS transistor

# 7. Package outline

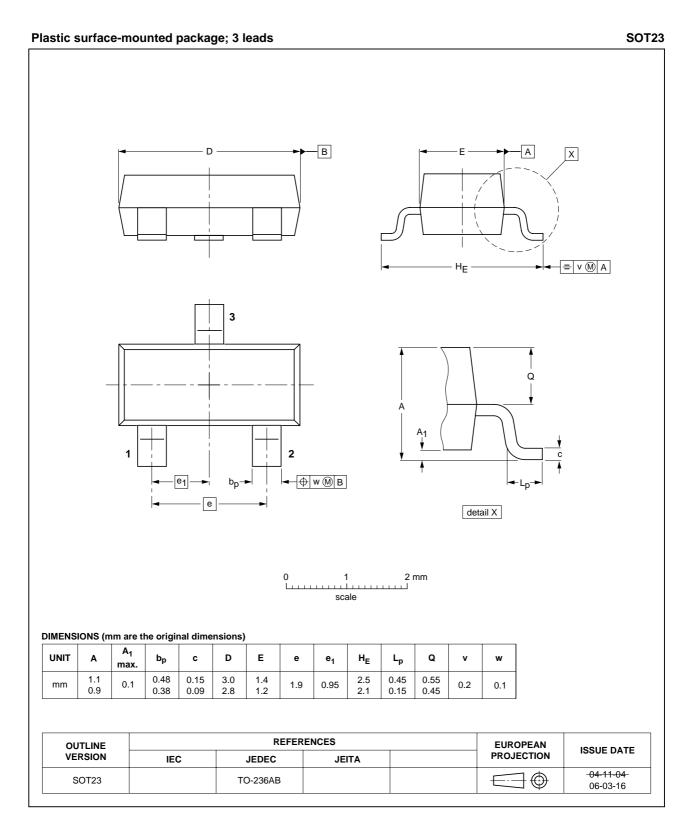


Fig 12. Package outline SOT23 (TO-236AB)

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## P-channel enhancement mode vertical D-MOS transistor

# 8. Revision history

## Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BSS84_4	20070717	Product data sheet	-	BSS84_3
Modifications:		of this data sheet has been red f NXP Semiconductors.	esigned to comply v	vith the new identity
	<ul> <li>Legal texts h</li> </ul>	nave been adapted to the new	company name whe	re appropriate.
	<ul> <li>Marking cod</li> </ul>	e has been removed.		
BSS84_3 (9397 750 11693)	20030804	Product specification	-	BSS84_2
BSS84_2 (9397 750 02333)	19970618	Product specification	-	BSS84_1
BSS84_1	19950407	Product specification	-	-

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# 9. Legal information

#### 9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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